

1 47225/PYI/V165

DIGITAL CLOCK RECOVERY SYSTEM

ABSTRACT OF THE DISCLOSURE

5 A digital clock recovery circuit. The digital clock
recovery circuit uses a lumped delay line and a digital phase
detector to form a recovered clock signal. The recovered
clock signal is limited to one clock period of the delay line
10 so as to prevent false locking.

DMC:PYI:rmw

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